

region includes a region from a minimum horizontal direction address to a maximum horizontal direction address among said addresses being accessed.

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10. (New) The medium of claim 8, wherein said image data region includes a substantially rectangular region from minimum vertical and horizontal direction addresses to maximum vertical and horizontal direction addresses among said addresses being accessed.

REMARKS

The Office action of January 13, 2003 has been received and its contents carefully noted.

Claims 1-4 are pending in the application. New claims 5-10 have been added.

Claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kuwajima et al. ("Kuwajima") (U.S. Patent No. 6,339,422) in view of Tsai et al. ("Tsai") (U.S. Patent No. 6,295,053). Applicants respectfully traverse these rejections, and request allowance thereof in the continuation prosecution application for the following reasons.

**The Claims are Patentable Over the Cited References**

**Combination of Kuwajima and Tsai is Improper**

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103, the rejection must identify some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the cited references. *MPEP §§ 706.02(j), 2142.* When the motivation to combine the references is not immediately apparent, it is the duty of the examiner to explain why the combination of the references is proper. *MPEP § 2142.* Additionally, the mere fact that references can be combined does not support a proper obviousness rejection unless the desirability of the combination is also suggested in the prior art. *Id.*

Applicants strongly contend that these MPEP requirements are not met by the rejection of claim 1 as the combination of the Kuwajima and Tsai references is improper since there lacks any suggestion or motivation to combine these two references. Kuwajima solely describes a method and system for providing a single clock source for a display circuit to reduce the frame (update) frequency (for a display device) and associated power consumption (see FIG. 3; Abstract, col. 2, lines 45-51; col. 4, lines 26-67; col. 5, lines 1-60). A variable frequency

controller divides a clock signal (generated from the single clock source) to reduce the frame frequency (speed) of retrieving image data from memory (for display on a display device) to reduce power consumption.

In contrast, Tsai solely describes a method and system for reprogramming video monitor functions using a programmable monitor controller that reads VGA (video graphic adapter) signals to initiate modification of monitor functions without having to manually change settings by opening the monitor casing (see FIGs. 3, 5; Abstract; col. 2, lines 17-60). The monitor controller includes a signal detector to detect commands carried by the VGA signals (generated by a VGA card) to activate monitor function modification (see col. 4, lines 66-67; col. 5, lines 1-10). Therefore, it would not be obvious to combine Kuwajima with Tsai since Kuwajima describes reducing the frame (update) frequency for displaying image data on a display device using a variable frequency divider which is a vastly different subject matter from Tsai's disclosure of a reprogrammable monitor controller to change video monitor functions.

Kuwajima is solely directed towards reducing the clock signal frequency for a display circuit to reduce the speed of image data retrieval (and display) from memory by a memory controller, while in contrast, Tsai is not directed towards image data retrieval from memory (nor the speed of image data

retrieval), but instead is solely directed towards monitoring and detecting control signals generated from a VGA card to initiate changing of monitor functions. Therefore, due to the significant distinction in subject matter presented by these two references, it would not be obvious to combine the variable (image) frame frequency system of Kuwajima with the reprogrammable monitor control system of Tsai.

**Claim 1 is not made obvious in view of Kuwajima and Tsai**

Claim 1 stands rejected under § 103(a) in view of Kuwajima and Tsai. Applicants strongly contend that both Kuwajima and Tsai, either alone or in combination, fail to disclose the features recited in this claim such as a write region detection means responsive to addresses accessed by the image data writing means for detecting a region including all the addresses, wherein when the image data writing means issues a transfer command, said transfer means transfers to the display means only such data that is in the region detected by said write region detecting means.

Neither Kuwajima nor Tsai disclose this patentably distinct feature of a write detection means for detecting a region including all the addresses accessed by an image data writing means, and wherein a transfer means transfers to a display means only such data contained within said detected region when receiving a transfer command from the image data writing means.

In contrast, Kuwajima solely describes a method and system for providing a single clock source for a display circuit to reduce the frame (update) frequency (for a display device) and associated power consumption (see FIG. 3; Abstract, col. 2, lines 45-51; col. 4, lines 26-67; col. 5, lines 1-60). A variable frequency controller divides a clock signal (generated from the single clock source) to reduce the frame frequency of retrieving image data from memory (for display on a display device) to reduce power consumption.

Specifically, Kuwajima discloses a display circuit including a VRAM controller, a CPU interface, and a display device interface wherein a VRAM, interconnected to the VRAM controller, contains display data to be displayed on a display device (see FIG. 3; col. 4, lines 61-62; col. 5, lines 1-21). Also, Kuwajima specifically states that "...display device interface outputs to the display device the binary display data via the VRAM controller based on the value stored in the display mode switching register [either binary display mode or gray-scale display mode] based on a display control signal." (see col. 6, lines 16-19). Thus, Kuwajima solely transfers all image data from memory (as requested by a display control signal) to a display device without any mention (as admitted in the Office Action) of the claimed write region detection means for detecting a region including all the addresses accessed by a image data

writing means and transferring only data within said detection region. Therefore, it is clear that Kuwajima does not disclose the recited feature making the claimed invention patentably distinct and non-obvious from Kuwajima.

Similarly, Tsai does not disclose the recited feature. In contrast, Tsai solely describes a method and system for reprogramming video monitor functions using a programmable monitor controller that reads VGA (video graphic adapter) signals to initiate modification of monitor functions without having to manually change settings by opening the monitor casing (see FIGs. 3, 5; Abstract; col. 2, lines 17-60). The monitor controller includes a signal detector to detect commands carried by the VGA signals (generated by a VGA card) to activate monitor function modification (see col. 4, lines 66-67; col. 5, lines 1-10).

Specifically, Tsai states that "...when erase/record commands are detected by the signal detector, the erase/record commands are re-directed to a ROM erase/record command decoder...signal detector taps the signals on the signal line SDA continuously, trying to match a pre-set address sequence...when the tapped consecutive address sequence matches that of the pre-set address sequence, a Set signal is sent to a monitor-in-system programming control flag unit ...indicat[ing] that reprogramming of the monitor system is desired..." (see col. 5, lines 4-7, 38-45). Thus, Tsai solely looks for a pre-set address sequence with a control data

stream to initiate monitor reprogramming (sending the erase/record commands to a decoder) which is in significant contrast to the recited write region detection means that detects an (image) region including all the addresses accessed by a image data writing means, and a transfer means that transfers only the data within said detection region to a display means when issued a transfer command from the image data writing means. Therefore, Tsai solely discloses a system that looks for predetermined control signals (address sequences) to initiate monitor reprogramming (decoding and execution of erase/record commands) which is significantly distinct from the recited write region detection means that detects an (image) region including all the addresses accessed by a image data writing means, and a transfer means that transfers only such data within said detected region when issued a transfer command from the image data writing means. Therefore, it is clear that both Kuwajima and Tsai, either alone or in combination, do not disclose the recited feature making the claimed invention patentably distinct and non-obvious from both references.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "VERSIONS WITH MARKINGS TO SHOW CHANGES MADE."

Conclusion

In view of the amendments and remarks submitted above, it is respectfully submitted that all of the remaining claims are allowable and a Notice of Allowance is earnestly solicited.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayments to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

The Examiner is invited to contact the undersigned at (703) 205-8000 to discuss the application.

Respectfully submitted,

BIRCH, STEWART, KOLASCH, & BIRCH, LLP

By Clint Gerdine  
Clint Gerdine  
(Reg. No. 41,035)

MKM/CAG:tm  
1190-0498P

P.O. Box 747  
Falls Church, VA 22040-0747  
Phone: (703) 205-8000

Attachment: Version with Markings to Show Changes Made

**VERSIONS WITH MARKINGS TO SHOW CHANGES MADE**

In the Claims:

Claims 5-10 have been added.